# High Temperature Precision Amplifier

Bruce W. Ohme
*Honeywell*
*bruce.ohme@honeywell.com*

Mark R. Larson
*Honeywell*
*mark.r.larson@honeywell.com*

Steve R. Erickson
*Honeywell*
*steve.r.erickson@honeywell.com*

## Abstract

Signal conditioning amplifiers are needed for down hole oil and gas data acquisition, especially for buffering high-impedance sensors. A dual high-temperature precision amplifier has been developed for down hole instrumentation, offering very low input offset voltage and drift, and 1/f noise suppression. The amplifier has been developed as a commercial, standard product offering in a ceramic DIP package, meeting requirements for operation from -55° to 225°C. All necessary auto-zero clock signals are generated internally, and no external capacitors are needed. The amplifier is completely self-biasing. Offsets at 250°C are typically less than 10 micro-volts, and input noise from 0.1 to 10 Hz is typically 5 micro-volts pk-pk. This makes this amplifier suitable for input conditioning for high-resolution DC or low-frequency applications. This design has been developed under the U.S. Dept. of Energy Deep Trek program.

## 1. Introduction

Signal conditioning amplifiers are needed in down-hole oil and gas data acquisition tools, especially for buffering high-impedance sensor outputs. Many applications involve DC-coupled sensors. When used in high-resolution data acquisition systems, low input offset current, very low offset voltage and good low-frequency noise response are primary considerations. For High-Temperature High Pressure (HTHP) wells these characteristics must be maintained at the high-temperatures encountered down hole.

Bulk CMOS amplifiers for high-temperature applications have been demonstrated [1-3]. One of these specifically addresses low-input offset voltage [4], reporting less than 200μV of offset voltage and 1nA of leakage up to 200°C. In general these require special design technique and expertise to overcome leakage and/or latch-up issues at high-temperature using bulk CMOS. It seems that there are no bulk-CMOS commercial offerings with established long-term reliability for temperatures above 200°C. More recently, activity in high-temperature amplifiers and signal conditioning circuits has exploited the superior high temperature behaviour of SOI CMOS to reduce leakage and eliminate device latch-up. [5-7]. However, the specific issues of low input offset voltage (and current), and low 1/f noise for DC/low-frequency applications have not been fully addressed in SOI CMOS.

This paper reports results for an SOI CMOS precision amplifier chartered by the High-Temperature Electronics Project under the U.S. Department of Energy (DOE) DeepTrek program. This program targets high-temperature electronic components needed for the development of very-deep HTHP oil and gas reserves. Industrial partners are involved in this program as a Joint Industrial Participation (JIP) consortium. The JIP prioritizes component development and determines target specifications. For this precision amplifier JIP development priorities are very-low input offset voltage and current, low noise especially for DC to 100Hz. signals, long-life and high reliability, and operating temperature range to at least 225°C (ambient). In addition, power consumption should be kept to a minimum. This should be achieved without reliance on external components (especially capacitors that are hard to find for these operating temperatures). It is a primary DOE objective that the components developed under this project should be available as commercial offerings at the conclusion of the program.

## 2. Design and Application Considerations

As with all of the components that are being developed under the DeepTrek High Temperature Electronics program, this development was completed using a partially-depleted High-Temperature SOI (HTSOI) CMOS process [8]. This

is a 0.8μ, 5-volt process that includes optional linear capacitor implant, lateral PNP bipolar transistor for reference/bias current generation, and thin-film CrSiN resistors. The SOI characteristics are used to achieve low-leakage and low-input bias current at high temperature. This technology has a track record of proven reliability for high-temperature applications. To achieve long operating life of the on-chip inter-connect (primarily aluminium) maximum current-density rules are applied to the layout.

Means for continuous compensation of offset-voltage and 1/f noise are required. A ping-pong architecture was selected which does not require that the auto-zero clock frequency is higher than the input signal bandwidth. Therefore, the amplifier may be used for applications beyond DC coupled/low-frequency signal conditioning. It is still the case that the output signal spectrum will have some content at the clock-frequency. Depending on the input signal and/or system application it is not clear if this is an issue. In any case, it is very desirable that clock-generation for offset compensation should be accomplished on-chip. Any capacitors required for offset compensation should be provided on-chip.

Power management is a trade-off vs. many other performance characteristics (such as drive current, slew-rate, bandwidth, etc.). Since many applications require only periodic measurement, duty-cycling may be used as a means to manage power without significantly compromising other parameters. Therefore it was decided to implement a "shutdown" feature to put the entire amplifier in a low-current mode with a high-impedance output.

A dual amplifier configuration was chosen for development. The project also included developing a custom package layout optimized for low-offset and isolation of the inputs between amplifiers and from digital noise. At the same time, it is expected that wafer/die level screening at high temperature will support delivery in die form. The intention is that this shall be a fully independent component suitable for production manufacturing including incorporation of ESD protection, short-circuit current limit, and capability for driving reasonable resistive or capacitive loads. A summary of the design goals arrived at by consensus among the JIP partners is shown in Table 1.

**TABLE 1 : Precision Amplifier Design Targets for -55°C to 225°C**

| Parameter | Target Value |
|---|---|
| Input Offset Voltage | 100 μV maximum |
| Mean Input Offset Voltage Drift | 0.2 μV/°C maximum |
| Input Bias Current @ 225°C | ±150 nA, |
| Input Offset Current @ 225°C | ±1nA, |
| Input Noise Voltage RS=100Ω, 0.1Hz – 10Hz | 3 μV pk-pk |
| Input Noise Current @ 225°C | 1.0 pA/√Hz |
| Input Range | $V_{SS}$ to $V_{DD}$ -2.0 |
| Common Mode Rejection Ratio (DC) | 100 dB, minimum |
| Power Supply Rejection (DC) | 100 dB, minimum |
| Large Signal Voltage Gain (DC); RL = 10kΩ | 100 dB, minimum |
| Gain-Bandwidth Product; RL = 10kΩ, CL = 20pF | 2.0 MHz |
| Slew Rate; RL = 10kΩ | 1.5 V/μs (typical) |
| Output Source/Sink (swing to 0.3V from either rail) | ±20 mA |
| Output Short-Circuit Current Limit | ±50 mA |
| Operating Supply Range | 5.0 Volts, ±5% |
| Supply Current, Total Package | 5.0 mA, maximum |
| Supply Current with Shutdown asserted | 150 μA, maximum |

## 3. Implementation

The ping-pong architecture follows that described by Opris and Kovacs [9]. Operation is illustrated in Figure 1. The ping-pong amplifier consists of two matched transconductance input amplifiers, A1 and A2. Each amplifier contains a primary pair of differential inputs, an auxiliary pair of differential inputs, and a single-ended output. The primary inputs handle the externally applied input signals, while the auxiliary inputs handle the internal offset voltage correction signal. Capacitors C2 and C4 store the offset correction voltages for A1 and A2, respectively, while capacitors C1 and C3 store a reference voltage level. A two-phase, non-overlapping clock provides the necessary switch timing.

A1 and A2 are alternately auto-zeroed: When A1 is being auto-zeroed, A2 is switched into the main signal path and provides amplification; when A2 is auto-zeroed, A1 is switched into the main signal path and provides amplification. Thus, the overall amplifier "ping-pongs" between A1 and A2, providing a continuous signal path from input to output.

The outputs of A1 and A2 are alternately switched to a common output node C, which in turn is connected to an output buffer stage A3, which provides the overall amplifier output. A3 provides rail-to-rail output swing with ±50mA drive capability over temperature.

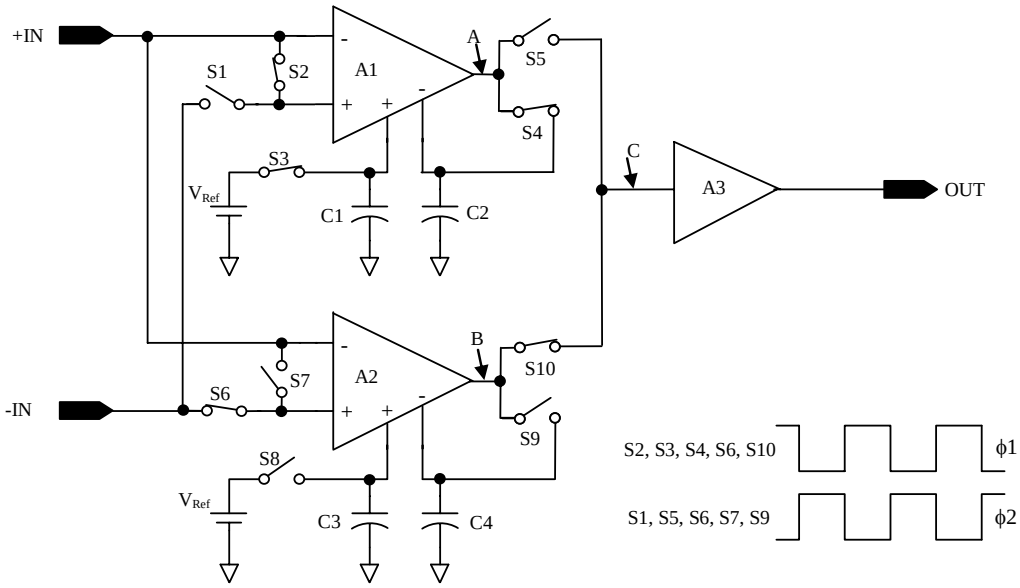



**FIGURE 1 : Ping-Pong Amplifier Block Diagram**

Figure 1 shows A1 being auto-zeroed, while A2 is "online" as the main signal amplifier. When A1 auto-zeroes, S2 closes, shorting together the main inputs of A1. S1 simultaneously opens (preventing the input terminals from shorting), while S3 and S4 also close. S3 connects a voltage reference to A1's (+) auxiliary input, while S4 connects A1's output, node A, to the (-) auxiliary input. This creates a unity-gain feedback loop and node A goes to approximately Vref. C2 charges to this voltage.

At the end of the auto-zero cycle, S3 and S4 open, storing the reference voltage and offset correction voltage on capacitors C1 and C2, respectively. The difference between the voltages on these capacitors ($V_{C1} - V_{C2}$) is the offset correction voltage, and is applied directly to the auxiliary differential inputs. A1 has now been auto-zeroed. The auto-zero procedure for A2 proceeds in an identical manner. This block diagram serves to describe the operation of the Ping-pong amplifier. However, it is a simplified block diagram in that additional circuitry to reduce switching transients at the output is not shown.

Note that the SOI technology is a key enabler for this design. A primary limitation in the offset accuracy is the leakage on the offset/reference storage capacitors. In this symmetrical architecture C1 and C2 experience similar magnitude of leakage, and thus the drift at the auxiliary inputs is largely common mode rather than differential. It is also highly beneficial that on-chip SOI switches and capacitors have much lower leakage than they would in a bulk technology.

A block diagram of the complete chip, the die layout, and the 14-pin DIP pin assignment are shown in Figure 2. The amplifier chip is completely self biasing. Within the bias generator block is a current source that provides PTAT (Proportional To Absolute Temperature) bias currents to the amplifiers. The PTAT characteristic is derived in a conventional manner using lateral PNP bipolar transistors operated at different current densities. This develops a $\Delta V_{be}$ mismatch between the two devices that has a PTAT characteristic. This PTAT voltage is converted to current by replication across a thin-film CrSiN resistor using a feedback loop. The PTAT current is mirrored as needed around the chip to bias the amplifiers. By properly sizing the input devices within the amplifiers, they can be operated in weak-inversion where the transconductance (gm) is almost inversely proportional to temperature. At the same time, gm is roughly proportional to PTAT bias current, and thus remains nearly constant over temperature. Consequently, PTAT bias renders the overall amplifier bandwidth roughly independent of temperature so that uniform and stable operation is achieved over a very wide temperature range.

The amplifier is also completely self-contained in terms of clock generation for operating the amplifier switches. An on-chip R-C oscillator provides the time base for switching. High precision is not required. However, a general concern in using this architecture and of having the digital clock switching on the same chip is the amount of clock

noise that feeds through to the output, and the effect that it may have on the effectiveness of the offset compensation. To avoid discrete frequency spurs at the output, a frequency randomizer is part of the clock generation. The on-chip oscillator runs at a base frequency of roughly 4MHz. This is "randomized" using a pseudo-random sequence generator in the frequency divider chain resulting in a switching frequency that randomly varies between roughly 2KHz to 4KHz. This feature can be defeated (i.e., switching at a single discrete frequency) by the RND control signal.

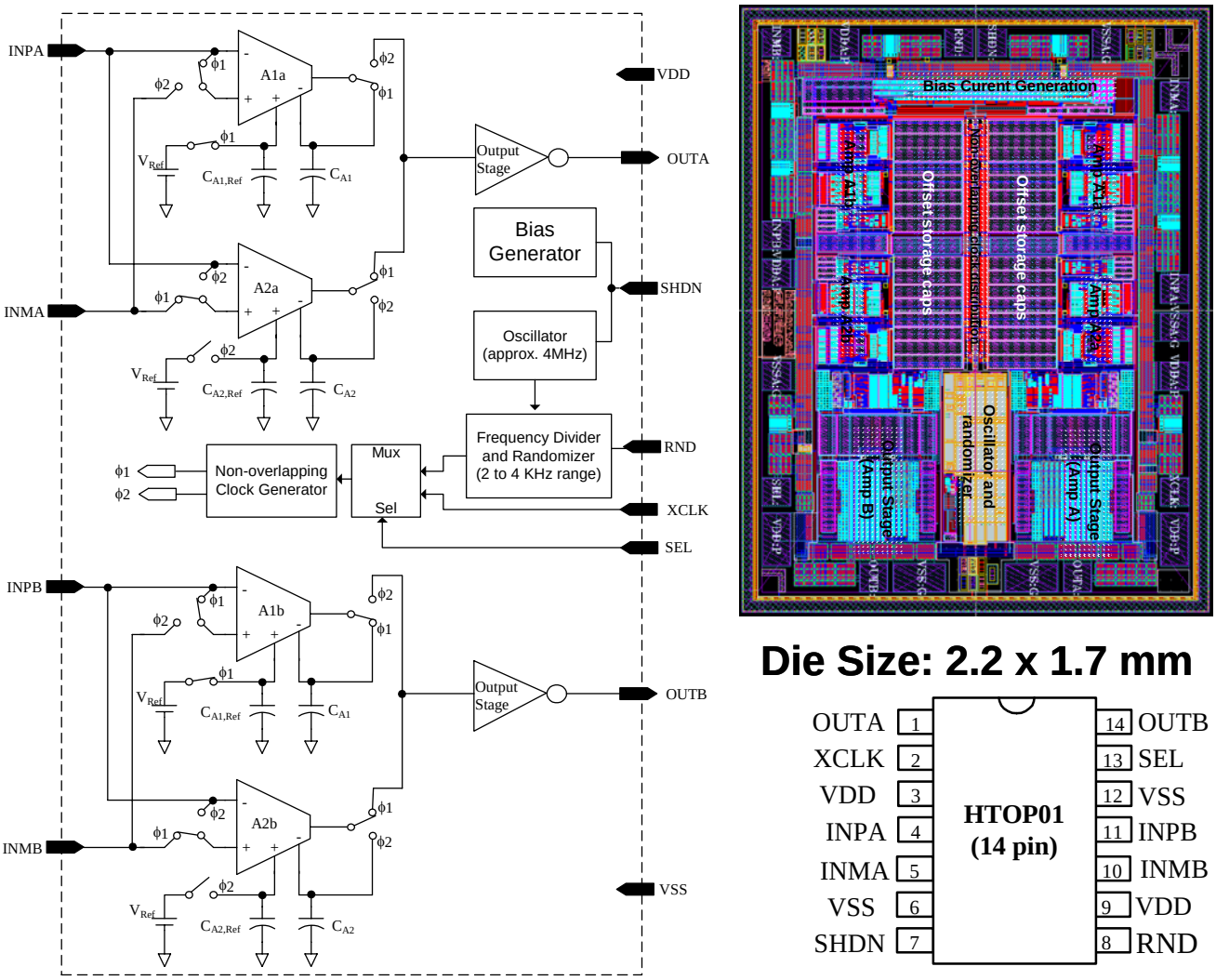



**Figure 2: Full-chip Block Diagram, Die Layout, and 14-pin DIP Pin-Out**

A "Select" pin provides means for selecting an external clock source in lieu of the on-chip clock. This may be advantageous in sampled data systems where the output of the amplifier is synchronously sampled by a down-stream component (e.g., an A-to-D). It also provides a convenient means for characterizing the amplifier response to different clock frequencies. Although not shown in the diagram, it is the case that when the external clock is selected, the internal oscillator and frequency divider are shut off. This makes it possible to determine the impact on accuracy of digital noise from on-chip clock generation relative to providing an off-chip clock source.

Careful attention was paid to layout for both the chip and the package. Digital functions are physically separated from the analog inputs, and on-chip power-supply routing is kept separate for analog and digital sections. ESD protection networks are matched and inter-digitated to reduce input leakage current mismatch as much as possible. The power-supply and output routing for the amplifier outputs are physically sized to handle the currents required without risk for failure from electro-migration at high temperature.

## 4. Results

A proof lot of the high temperature amplifier has completed fabrication and testing. Wafer probing was completed using a hot-chuck at 200°C centigrade, follow by package assembly in 14-pin DIP and automated testing at -55°C, 25°C, and 225°C (Thermo-stream® air temperature). This has been supplemented by laboratory bench testing for various parameters. Results are shown in Table 2 and Figure 3.

Automated offset voltage measurement of 47 packages using the internal clock verifies that offset voltage is within the 100µV target over the full temperature and input range. Bench testing on a sample basis shows that offset voltage performance is significantly improved by using an external clock. Typical measured offsets are less than 1µV at room temp. and within ±5µV over the full operating range when an external clock is used. Measurement of offset at these levels requires careful attention to the test set-up, especially using an external clock source. Sandia National Laboratory completed testing at 300°C (Figure 3a) after 438 hours of 300°C operation (117 hrs. in 5% hydrogen atmosphere). Results show the offset is still within 10µV up to about 2.25V input. Above 2.25V there is a curious spike in the offset voltage (up to 24µV) that is not yet explained. These results were obtained using an external clock at 3KHz.

The noise behaviour of the amplifier is also very interesting. Figures 3c and 3d show noise characteristics vs. temperature and clocking frequency respectively. It can be seen that the noise performance actually improves at 225°C relative to lower temperatures. Furthermore, it can be seen that low-frequency noise suppression is improved as the clock frequency increases from 1KHz. At about 30KHz. the 1/f noise is suppressed to approximately the wide-band channel noise level of the amplifier. Interesting noise characteristics are also observed (depending on test apparatus) when using the internal clock. Figure 3a used the internal clock and showed a flat noise response. Figure 3b also includes a curve using the internal clock but shows a peaking in the noise characteristic at about 100Hz. This remains to be fully explained. More testing will need to be completed to validate and refine these results.

**TABLE 2 : Selected Package Test Data** (-55°C to 225°C) unless noted

| Parameter | Target Value | Measured Results |
|---|---|---|
| Input Offset Voltage | ±100 µV (max.) | ±5 µV (external clock) |
| Supply Current (5.25V supply, 225°C) | 5 mA | 1.85 mA |
| Open-loop Gain (-55°C to 225°C) | > 100dB | > 114dB |
| Input Noise Voltage RS=100Ω, 0.1Hz – 10Hz<br>(internal clock)<br>(External clock at 30KHz) | 3 µV pk-pk | 5.7 µV pk-pk @ 23°C<br>4.6 µV pk-pk @ 225°C<br>1.4 µV pk-pk @ 23°C |
| Input Noise Current @ 225°C | 1.0 pA/√Hz | To be measured |
| Input Range | $V_{SS}$ to $V_{DD}$ -2.0 | $V_{SS}$ to $V_{DD}$ – 1.7 |
| Output Source/Sink (swing to 0.3V from either rail) | ±20 mA | > 20 mA |
| Output Short-Circuit Current Limit | ±50 mA | 51 mA (average) |
| Supply Current with Shutdown asserted | 150 µA, maximum | 13 uA, typical |

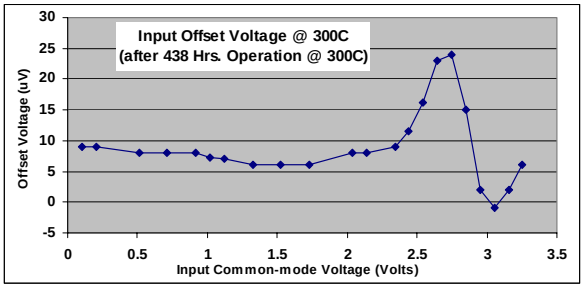



Figure 3a

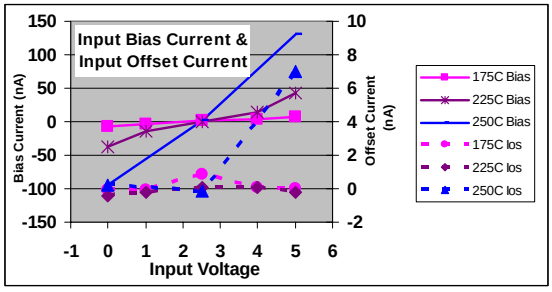
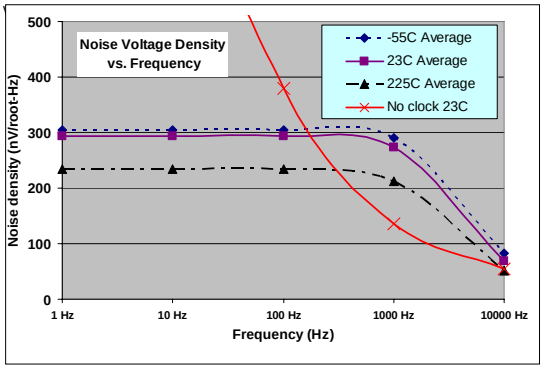



Figure 3b



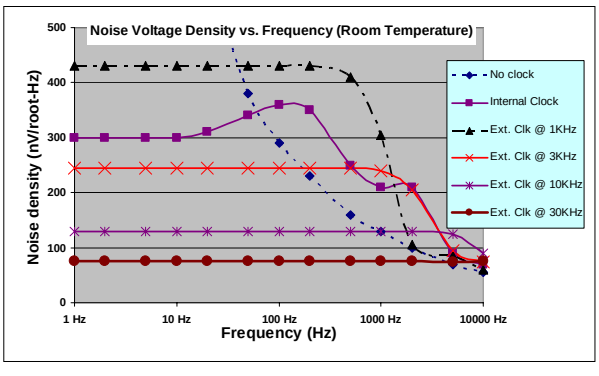



Figure 3c

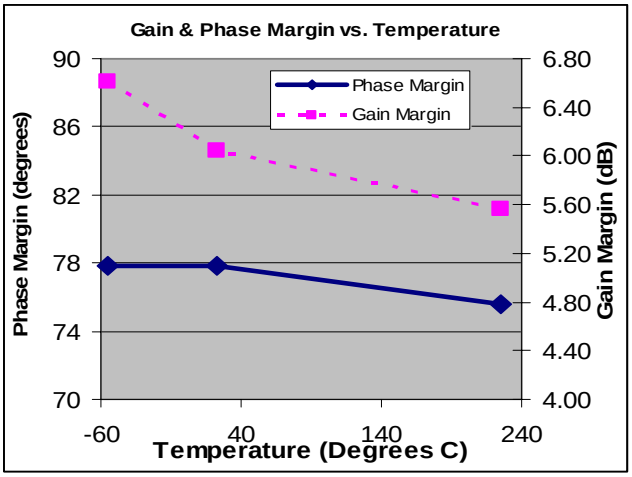



Figure 3e

Figure 3d

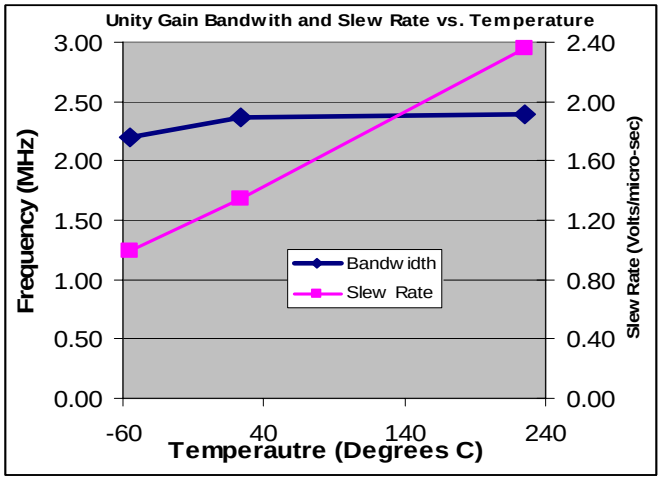



Figure 3f

## 5. Summary and Conclusion

A dual high-temperature precision amplifier requiring no external component has been successfully developed and demonstrated at temperatures ranging from -55°C to 300°C. Excellent offset performance, low offset drift with time and temperature, and effective suppression of 1/f noise make this amplifier suitable for use in high-temperature precision DC and/or low-frequency applications. However, it is apparent that performance is improved by using an external clock source at higher frequencies relative to the internal clock. This suggests that low-frequency noise suppression could be further improved by simple changes to the design (by increasing the internal clock frequency, for example).

## Acknowledgements

The authors would like to thank Joe Henfling and Randy Norman of Sandia National Laboratories for characterization test support (especially at 300°C). The authors also acknowledge the financial and technical support received from the National Energy Technology Laboratory (NETL), a facility of the U.S. Dept. Of Energy.; as well as financial and technical support of the Deep Trek Program Joint Industrial Participation (JIP) consortium. JIP members are: BP, Baker Hughes, Goodrich Aerospace, Halliburton, Honeywell, Novatek, Quartzdyne, and Schlumberger.

REFERENCES

1. Eggermont, J.P.; Gentinne, B.; Flandre, D.; Jepsers, P.; Colinge, J.P.; "SOI CMOS Operational Amplifiers for Applications Up To 300°C", Proceedings 2nd International High Temperature Elecrtronics Conference (HiTEC), Volume II, pp. 21-26. 1994.
2. Bergmann, J; ten Have, A, "High Temperature Operational Amplifier with Low Offset Voltage", Proceedings International Symposium on Signals, Systems, and Electronics, pp. 451-454. 1995.
3. de Jong, P.; Meijer, G.; van Roemund, A.; "A 300°C Dynamic-Feedback Instrumentation Amplifier", Proceedings International Solid-State Circuits Conference, pp. 322-323. 1998.
4. I. Finvers, J. Haslett, "A High Temperature Precision Amplifier", IEEE Journal of Solid State Circuits, Vol 30, No. 2, February 1995.
5. Demeus, L.; Dessard, V.; Viviani, A.; Adriaensen, S.; Flandre, D. "Integrated Sensor and Electronic Circuits in Fully Depleted SOI Technology for High-Temperature Applications" IEEE Transactions on Industrial Electronics, Vol. 48, No. 2. pp. 272-280.
6. www.hightempsolutions.com/datasheets/HT1104pdf, "High Temperature Quad Operational Amplifier" datasheet, Rev. B. September 2003.
7. Takao, H.; Ina, F; Douzaka, T.; Sawada, K.; Ishida, M.; "SOI-CMOS Precision Front-End Amplifier for Wide Range and High Tmperature (200°C) Operation of Smart Mircosensors", Sensors & Actuators A: Physical; May2004, Vol. 112 Issue 2/3, pp. 388-394.

8. Ohme, B.; Lucking, T.; Gardner, G.R.; Vogt, E.; Tsang, J.; “High Temperature 0.8 Micron 5V SOI CMOS for Analog/Mixed Signal Applications”, Proceedings 2004 IMAPS International Conference and Exhibition on High Temperature Electronics (HiTEC 2004). Session WA2, pp. 1-6. 2004.
9. Opris, I.; Kovacs, G. “A Rail-to-Rail Ping-Pong Op-Amp”. IEEE Journal Of Solid State Circuits, Vol. 31, No. 9. pp. 1320-1324. September, 1996.